VR4181 64-BIT MIPS RISC MICROPROCESSOR

FOR WINDOWS CE

The 64-bit VR4181™ (μPD30181) RISC microprocessor is an NEC VR Series™ device created specifically for Windows® CE-based palm-size PC/smart phone applications. Designed using the popular MIPS® RISC architecture and revolutionary Modular Bus Architecture (MBA), the VR4181 offers excellent power consumption and performance in a highly integrated, low-cost system-on-a-chip (SOC).

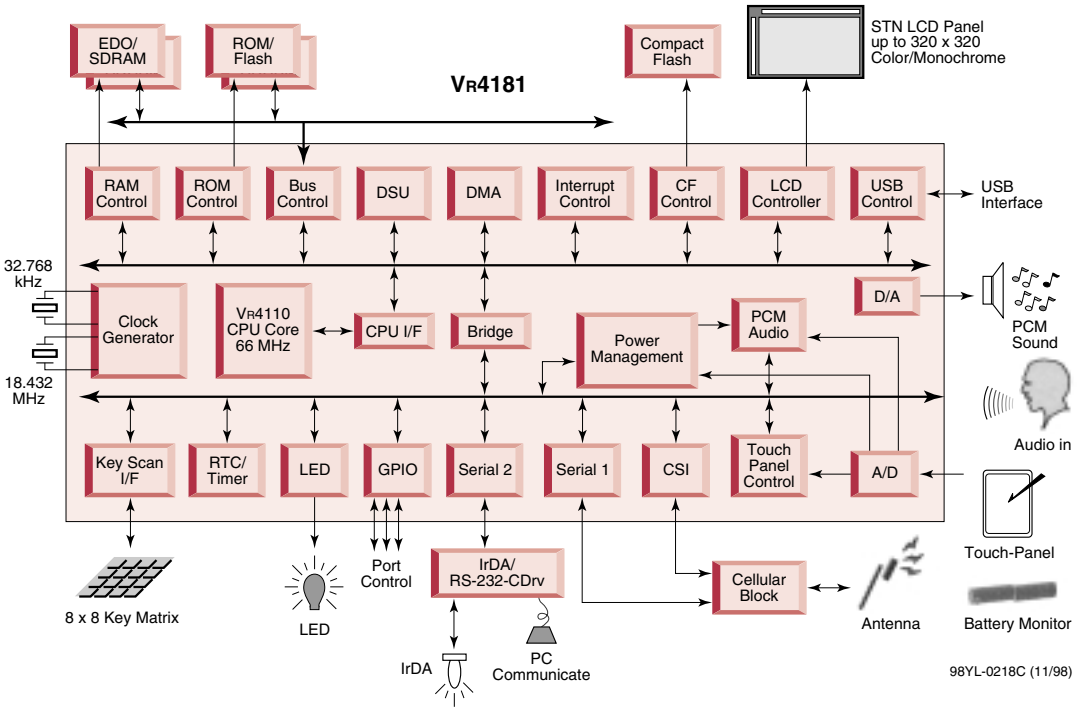
The VR4181 microprocessor is the second NEC device to use the ultra-low-power-consuming 66-MHz VR4110™ CPU core based on advanced 0.25-micron technology. The VR4110 CPU has an optimized five-stage pipeline, 4-KB instruction cache, 4-KB data cache, multiply-and-accumulate (MAC) unit, and memory management unit that enable high performance in a compact, low-cost chip.

The VR4181's integrated peripherals include an LCD controller, CompactFlash™ interface, power management unit, DMA unit, interrupt control unit, timers, real-time clock, one 16550-compatible serial interface, IrDA® 1.0 interface, keyboard interface, touch-panel interface, universal serial bus (USB) functional interface, A/D converter, and D/A converter.

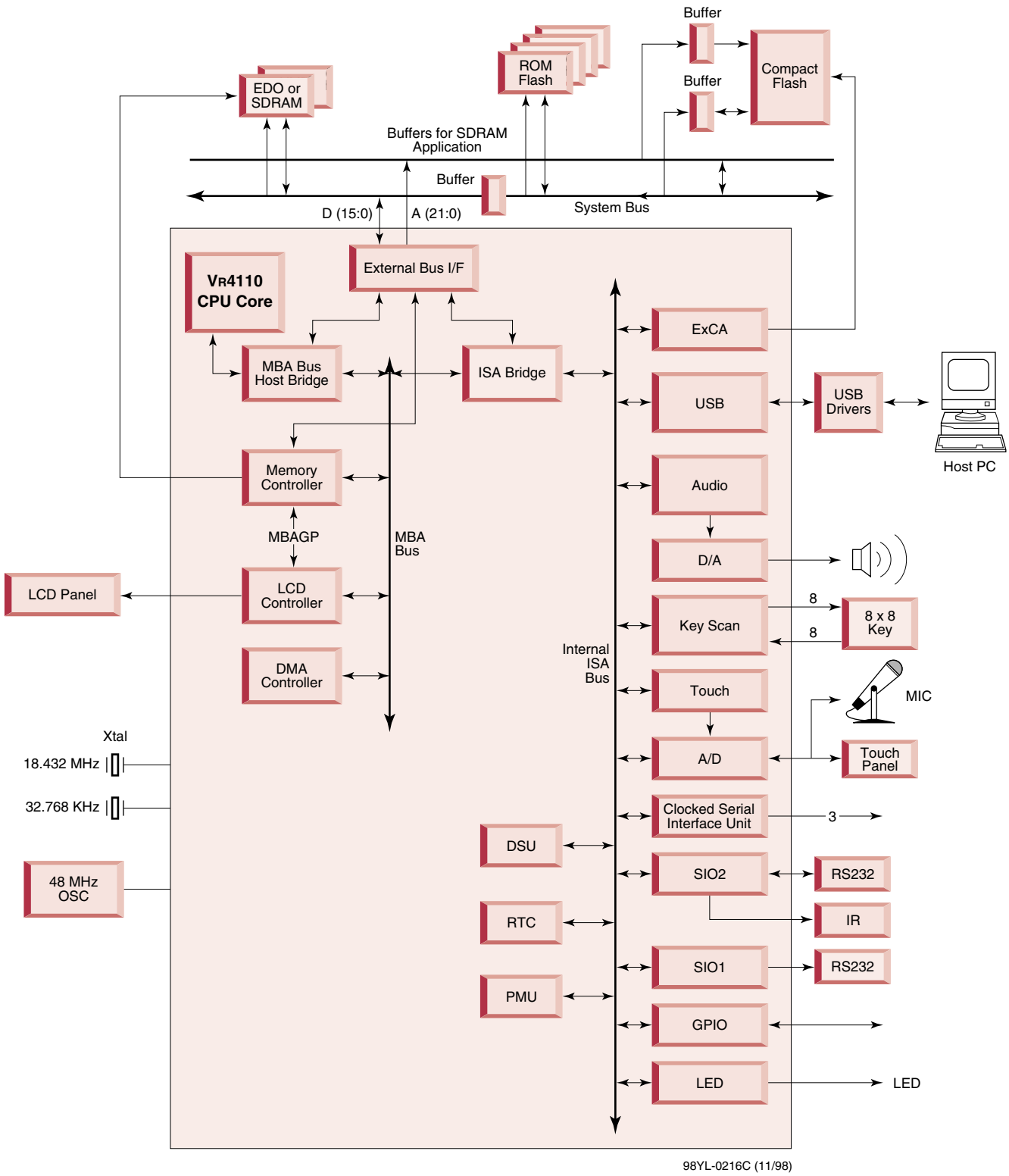
The VR4181 microprocessor complies with the MIPS I, II, and III instruction set architectures (ISAs) and MIPS16 application-specific extension (ASE). The MIPS16 ASE compliance enables the VR4181 to incorporate 16-bit-long instruction format with conventional 32-bit-long instruction support, which results in compact code size, smaller memory foot print, and lower system cost.

The VR4181 is an excellent choice for palm-size PC designers because its high performance, compact size, and low power consumption make it ideal for use in battery-driven, portable handheld systems.

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



FEATURES

VR4110 CPU CORE
— MIPS III ISA-compliant
— MIPS 16 ASE-compliant for compact code density (40% denser code than MIPS32)
— Five-stage pipeline running up to 66 MHz
— Single-cycle MAC instruction for digital signal processing operations

MEMORY MANAGEMENT UNIT
— 32-bit physical address range of 4 GB with 40-bit virtual address space
— 32 double-entry TLBs supporting 1~256 KB page sizes
— Up to 64 MB of SDRAM/EDO/fast-page DRAM and 64 MB of SROM/flash memory/mask ROM
— Up to 66 MHz operation

CACHE MEMORY UNIT
— 4-KB direct-mapped instruction cache
— 4-KB direct-mapped data cache
— Write-back cache for reducing store operations

BUS CONTROL UNIT
— Ultra-power-saving Modular Bus Architecture (MBA)
— 32-bit and 16-bit addressing modes
— Dynamic bus sizing supports subset of ISA bus

POWER MANAGEMENT UNIT WITH FOUR POWER-SAVING MODES
— Full speed
— Standby
— Suspend
— Hibernate

CLOCK GENERATOR UNIT
— Built-in PPL for frequency multiplication
— External bus frequency of 16 and 33 MHz

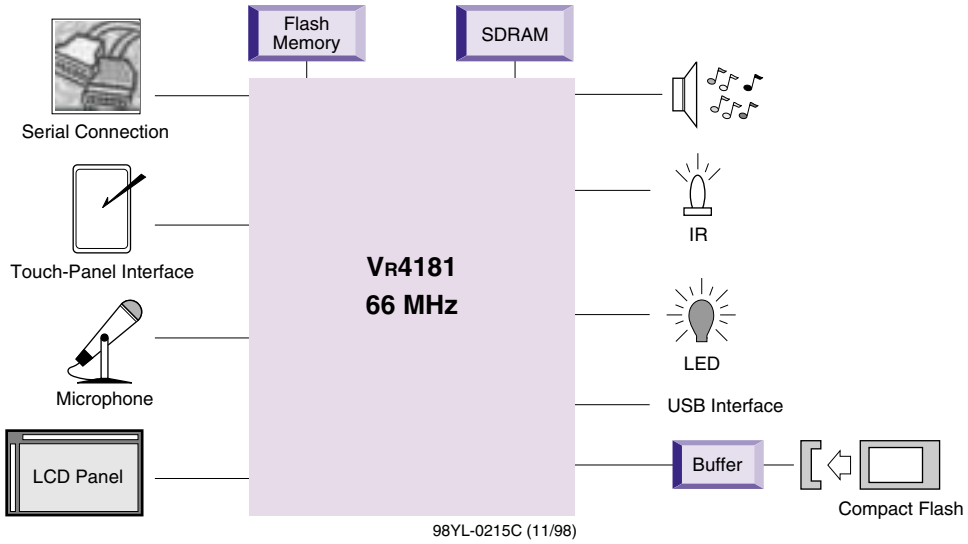
SERIAL INTERFACE UNIT
— One 16550-compatible channel
— RS-232C compliant
— Up to 115 kbps

OTHER PERIPHERALS
— **Real-time clock** with four built-in timers
— **Interrupt control unit** with internal and external interrupts
— **DMA address unit** and **DMA control unit** with four different channels
— **General-purpose I/O unit**
— 64-key **keyboard interface**
— 12-bit **A/D converter** for **touch-pannel interface** and **audio input**
— **Infrared unit:** IrDA 1.0 standard communication
— **Audio interface unit** and 10-bit **D/A converter** for **audio output** and **microphone input sampling**
— **USB** function interface: file/data synchronization with a desktop/laptop systems

AC/DC Specifications
— 66 MHz maximum frequency
— 2.5- and 3.3-volt operation
— <250-mW typical power consumption

PACKAGE
— Compact size: 16 x 16 x 1.3 mm
— 160-pin LQFP

PALM-SIZE PC IMPLEMENTATION



98YL-0215C (11/98)

ORDERING INFORMATION

PART NUMBER	PACKAGE	MAXIMUM OPERATING FREQUENCY
µPD30181GM-66-8ED	160-pin LQFP	66 MHz

VR4111, VR4121, AND VR4181 COMPARISON

	VR4111	VR4121	VR4181
CPU Core	VR4110	VR4120	VR4110
Max. Pipeline Clock	70 MHz	168 MHz	66 MHz
Cache Size	16K instruction cache 8K data cache	16K instruction cache 8K data cache	4K instruction cache 4K data cache
Performance	90 Dhrystone MIPS	215 Dhrystone MIPS	85 Dhrystone MIPS
Instruction Set	MIPS I, II, III MIPS 16	MIPS I, II, III MIPS 16	MIPS I, II, III MIPS 16
MAC Instruction	Single-cycle, 16-bit	Single-cycle, 32-bit	Single-cycle, 16-bit
Operating Voltage	2.5 V (core), 3.3 V (I/O)	2.5 V (core), 3.3 V (I/O)	2.5 V (core), 3.3 V (I/O)
Integrated Peripherals	Same	Same	Same plus: CompactFlash™ Interface LCD controller USB functional interface
Memory Interface	64 MB DRAM 64 MB ROM	64 MB DRAM 64 MB ROM	64 MB DRAM 64 MB ROM
Power Consumption	185 mW	300 mW	250 mW
Package	224-pin FPBGA	224-pin FPBGA	160-pin LQFP
Process Technology	0.25-micron UC2 process	0.25-micron UR2 process	0.25-micron UC2 process

NEC

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